interrupter but disposed outside of a processor such as processor **100**. Shift register **505** can extend across multiple processor half cycles such as **120** processor half cycles and can include multiple recorded bits such as a recently recorded bit **509** and a last recorded bit **511**. When a recently recorded bit **509** is inserted into a shift register, then a last recorded bit **511** drops off.

[0165] FIG. **5**C also shows that across a third time period or an arcing window, multiple processor half cycles can be read or analyzed to determine the presence of an arc during a third time period or arcing window. For example, FIG. **5**D shows a first type of arcing window **516** which is based upon a predetermined time period such as 1 second. FIG. **5**E shows a second type of arcing window **517** which is based upon a second predetermined time period, while FIG. **5**F shows a third type of time period based upon another predetermined time period. For example, in a preferred embodiment the predetermined time period for arcing window **516** could be 1 second based upon a current reading such as reading **504** of less than 5 A. A predetermined time period for arcing window **517** could be 400 ms which could be based upon a current reading such as amplitude reading **504** of greater than or equal to 5 A but less than 10 A. A predetermined time period for arcing window **518** could be 200 ms which could be based upon a current reading of over 10 A.

[0166] Once processor **100** determines that there is an arcing fault, it would preferably send an interrupt signal to disconnect line side **11** from load side **70** (including downstream load and face load on receptacle), thereby cutting power between conductive paths **16** and **18** on the line side and load conductive paths **17** and **19**. Processor **100** is configured to cause interrupting mechanism **60** to disconnect the line side from the load side.

[0167] Generally, interrupting mechanism **60** may include a coil or solenoid **63**, a plunger **65**, an actuator circuit **61**, and any other additional elements or devices known in the art which may be configured to selectively interrupt electrical current on conductive paths **16** and **18** and selectively isolate power preferably between line side **11**, load side **70** and a set of face contacts such as those used for receiving a plug.

[0168] Alternatively, interrupting mechanism **60** may be arranged and configured to isolate selective conductive paths; e.g., line side **11** from load side **70**, or line side **11** from a set of face contacts, etc.

[0169] In at least one embodiment, there are first, second, and third electrical conductors where the first, second and third electrical conductors may be: (i) selectively isolated from each other and (ii) selectively connected to each other. Interrupting mechanism **60** is arranged and configured to selectively isolate the first, second and third electrical conductors from each other. Likewise, interrupting mechanism **60** may also be arranged and configured to selectively connect the first, second and third electrical conductors to each other.

[0170] Actuator circuit **61** may include SCR **61.1**, resistor R**19**, resistor R**12** and capacitor C**2**. Resistor R**12** and capacitor C**2** are used in one preferred embodiment and act as a filter circuit to prevent false triggering of SCR **61.1**. In addition, resistor R**23** and capacitor C**9** may be employed to act as a snubber circuit in order to reduce the noise in the circuitry to improve the triggering/firing capability and reliability of SCR **61.1**. Alternatively, a TVS circuit SI**1** can be electrically coupled between the coil **63** of actuator **60** and SCR **61.1**. Use of such a snubber circuit in certain preferred embodiments would be to improve the reliability of SCR **61.1**. The snubber circuitry shown in FIG. **3**A preferably minimizes overvoltage stress on the AFCI components/elements in the event of power line surges. Alternatively, to reduce overvoltage in the event of a surge, one or more bi-directional TVS diodes can be used in place of, or in addition to, RC snubber circuitry (see e.g., FIG. **3**C).

[0171] Advantageously, the combination of the TVS diodes and the trip coil inductance in the arrangement/configuration shown permits the trip coil to behave as a current limiting component for the TVS diodes. Such a configuration could help to reliably protect the AFCI components against surges and further does not exhibit some or all of the acoustic noises that may be associated with the RC snubber circuitry discussed above. To withstand abnormal overvoltage conditions, e.g., when input voltage jumps to double the normal power line voltage, the TVS circuitry should be designed/configured to withstand a 350V-400V nominal voltage range. One possible example of a TVS circuit/design is the commercially available SMBJ350CA offered by Littlefuse.

[0172] An SCR signal, denoted SCR, may be output by processor **100** from, e.g., pin P**7** to selectively activate SCR **61.1**. Actuation of SCR **61.1** causes coil **63** to be energized, resulting in movement of plunger **65** to selectively open contacts **62**.

[0173] FIG. **6**A is a perspective view of one representative embodiment of the AFCI circuitry in accordance with certain teachings of the present inventive features, shown in one or more of FIGS. **1**A-H and **3**A-**3**F. FIG. **7** shows housing **200**, which is configured to house the AFCI circuitry, e.g., any one of the disclosed circuits **6**, **6.1**, or **6.2**. AFCI circuitry includes but is not necessarily limited to sensors or transformers **22**, **24**, and **26**, line terminals **12** and **14**, separable contacts **64** and **66**, line side conductive paths **16** and **18** (not shown in this view), load side conductive paths **17** and **19**, and load terminals **72** and **74**. FIGS. **6**A and **6**B illustrate that in certain preferred embodiments of the invention the AFCI circuitry can be configured in a space saving manner allowing installation in a single gang enclosure, such as a single gang wall box/junction box, to create an in-line/branch circuit AFCI device.

[0174] While the sensors and the circuitry can be configured in any usable way on a circuit board, FIG. **6**B illustrates a side view of one possible configuration for a circuit board layout of any one of circuits **5**, **6**, **6.1**, or **6.2**. For example, the side view of circuit board **201** may preferably be configured to support, or be coupled to, much or all of the circuitry shown in FIGS. **1**A-**3**F. As shown in this view, there is disclosed a three sensor configuration, with two sensors being arranged on a first side and one other sensor being arranged on the opposite side. In certain preferred embodiments, differential transformer **26** may be nested inside of the inner perimeter of high frequency transformer **22** and low frequency current transformer **24** may be disposed on the opposite side of circuit board **201**. Any one of the sensors may be partially disposed within the thickness of board **201** rather than on either side as well. However, it should be readily understood that other configurations can also be used, such as those shown in FIGS. **1**A-**1**H. Advantageously, because stacking two or more sensors on top of each other may potentially require shielding resulting in the need for a